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(54) **MAGNETORESISTIVE ELEMENT AND METHOD OF MANUFACTURING THE SAME**

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H01L 43/02 (2006.01)
H01L 43/12 (2006.01)
H01L 43/08 (2006.01)

(52) **U.S. Cl.**

CPC ***H01L 43/12*** (2013.01); ***H01L 43/08*** (2013.01)

(58) **Field of Classification Search**

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See application file for complete search history.

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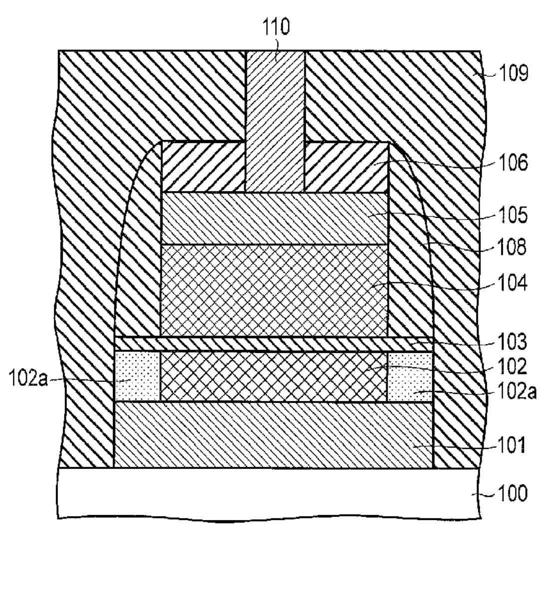
(57) **ABSTRACT**

According to one embodiment, a magnetoresistive element is disclosed. The element includes a lower electrode, a stacked body provided on the lower electrode and including a first magnetic layer, a tunnel barrier layer and a second magnetic layer. The first magnetic layer is under the tunnel barrier layer, the second magnetic layer is on the tunnel barrier layer. The first magnetic layer includes a first region and a second region outside the first region to surround the first region. The second region includes an element in the first region and other element being different from the element.

7 Claims, 5 Drawing Sheets



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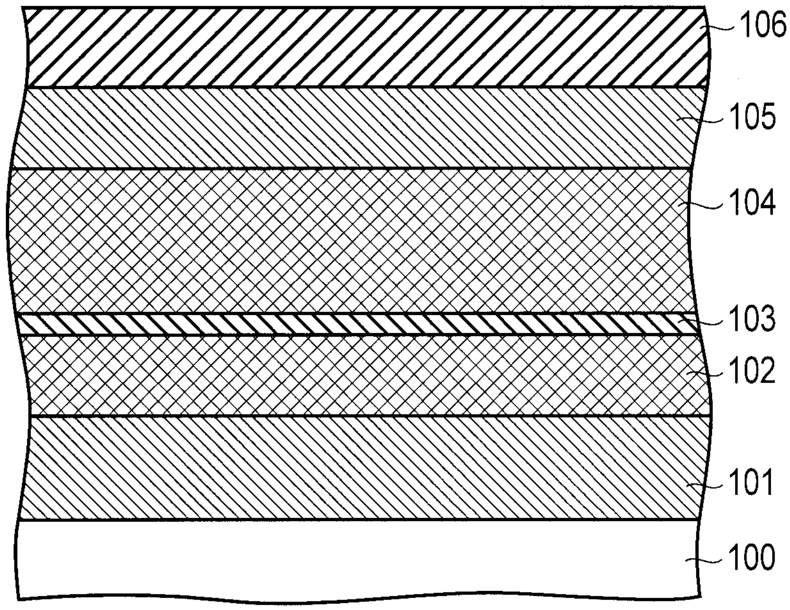

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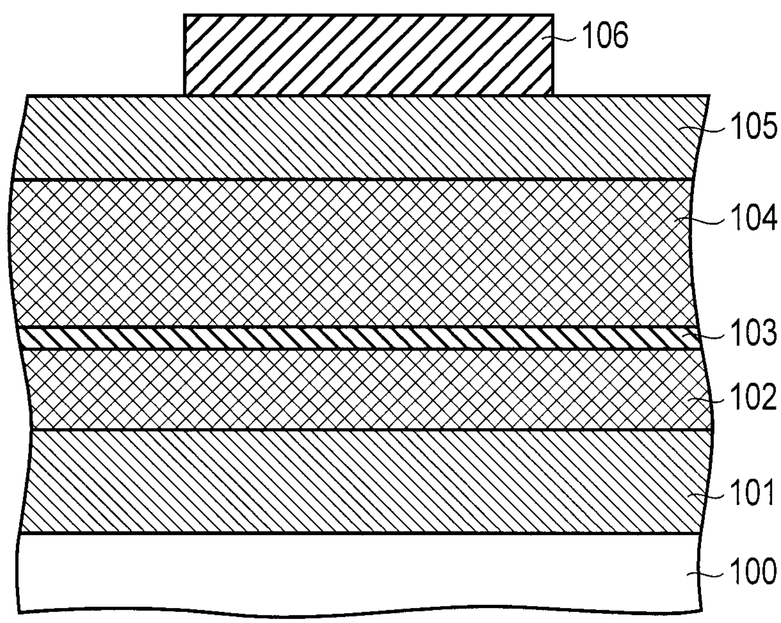

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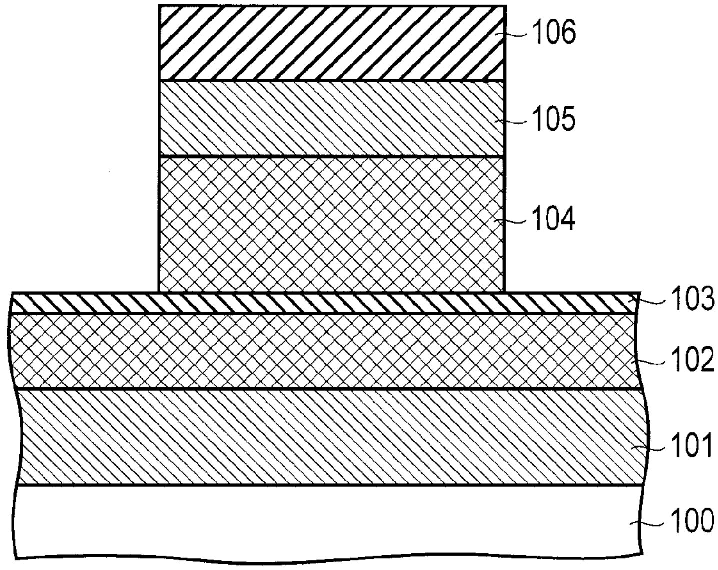
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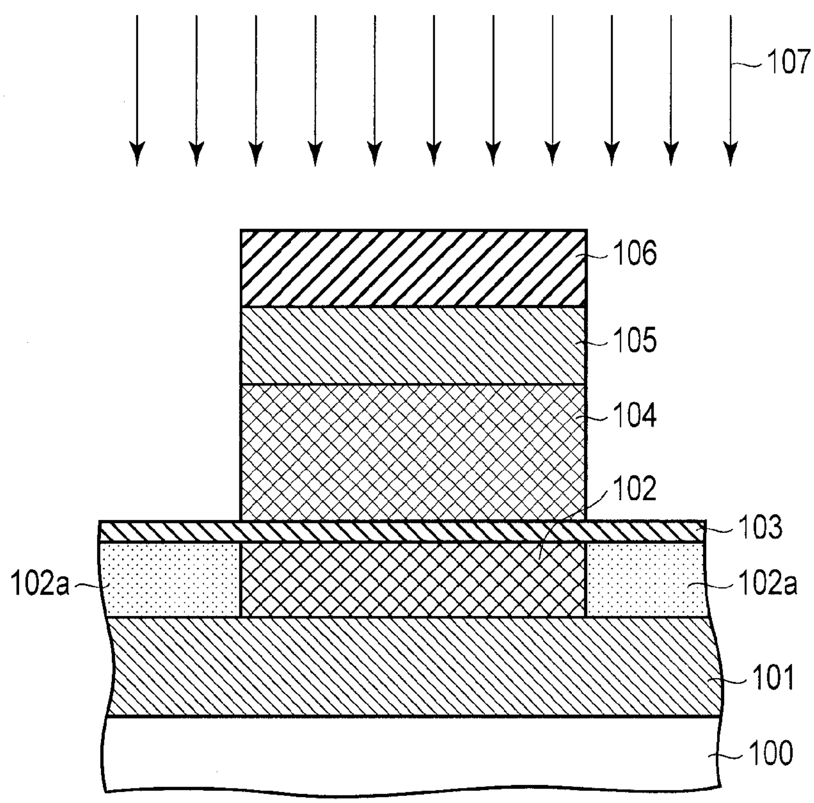
105
104
103
102
101
100

F I G. 3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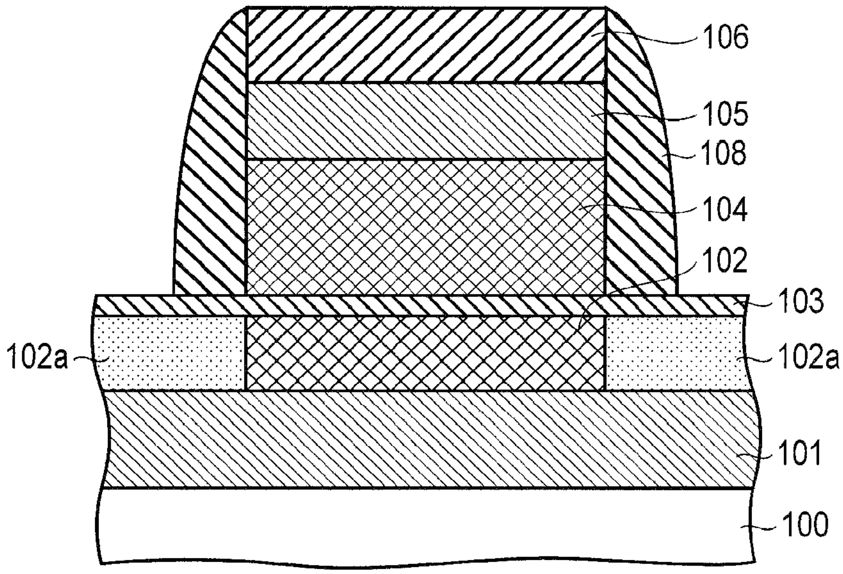
F I G. 4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102
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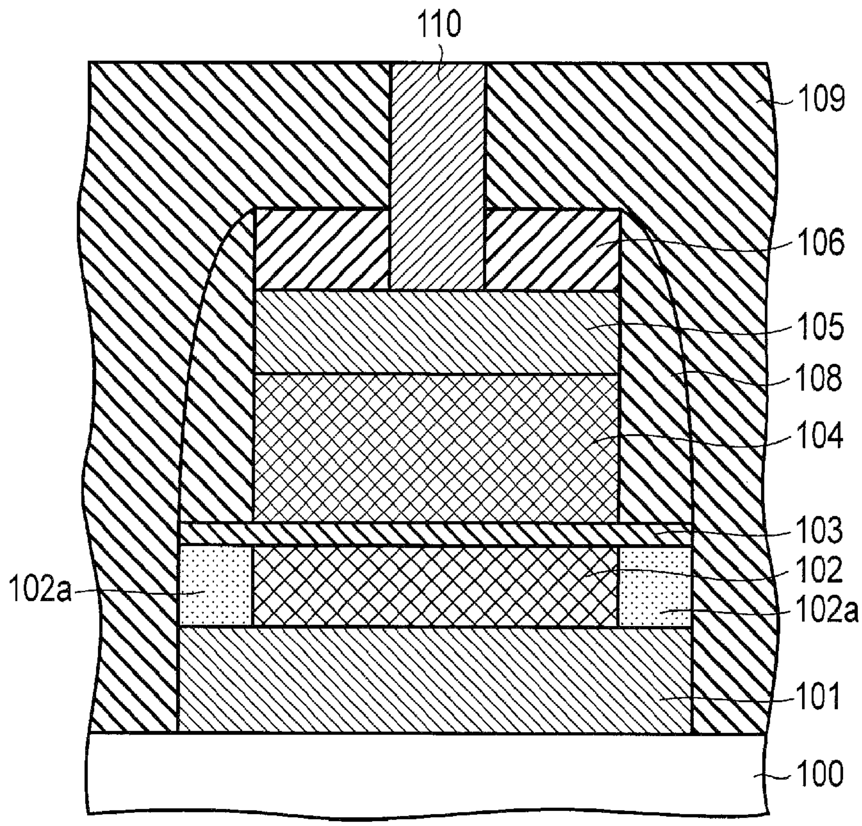
102a
101
100

F I G. 5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109
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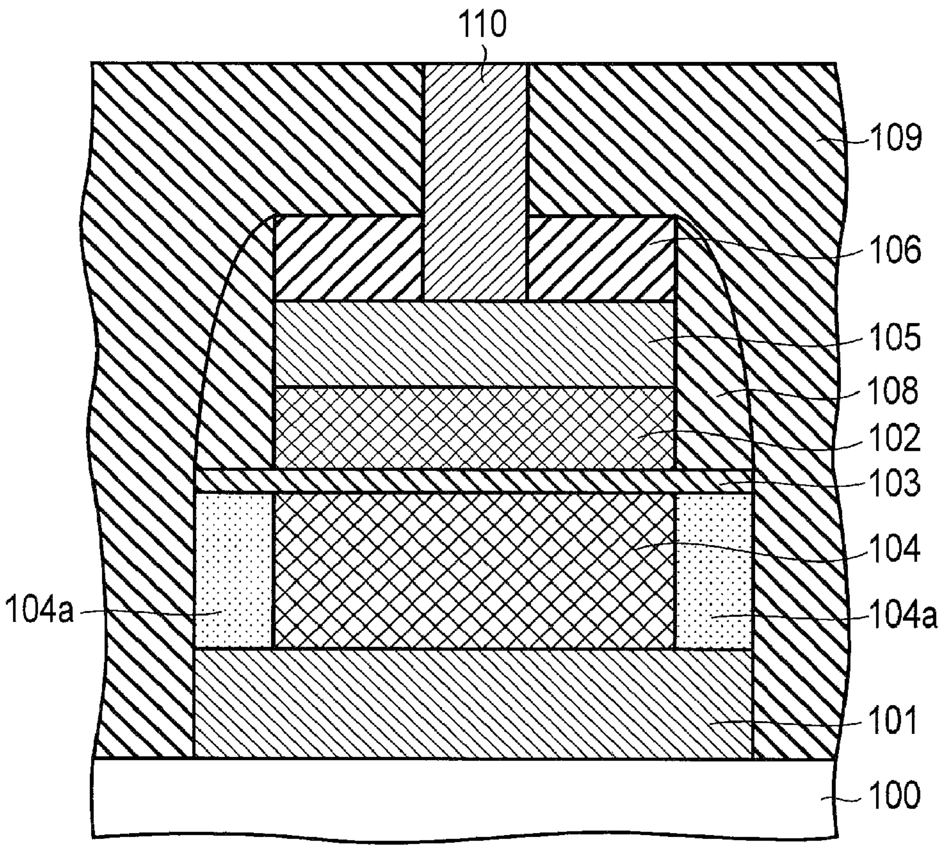
105
108
104
103
102
102a
102a
101
100

F I G. 6



F I G. 7

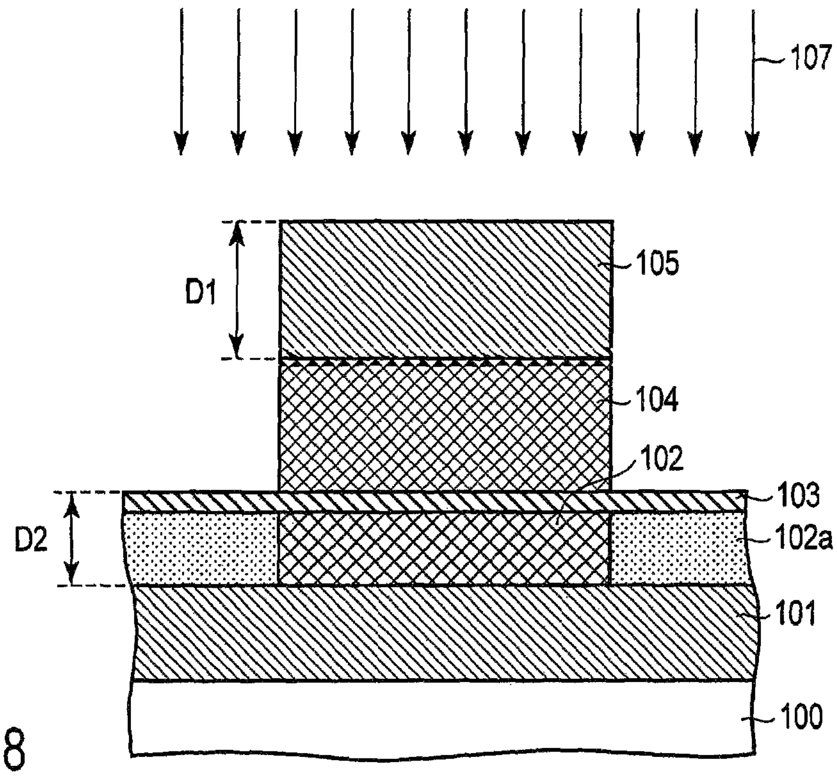

107
D1
105
104
102
103
D2
102a
101
100

FIG. 8

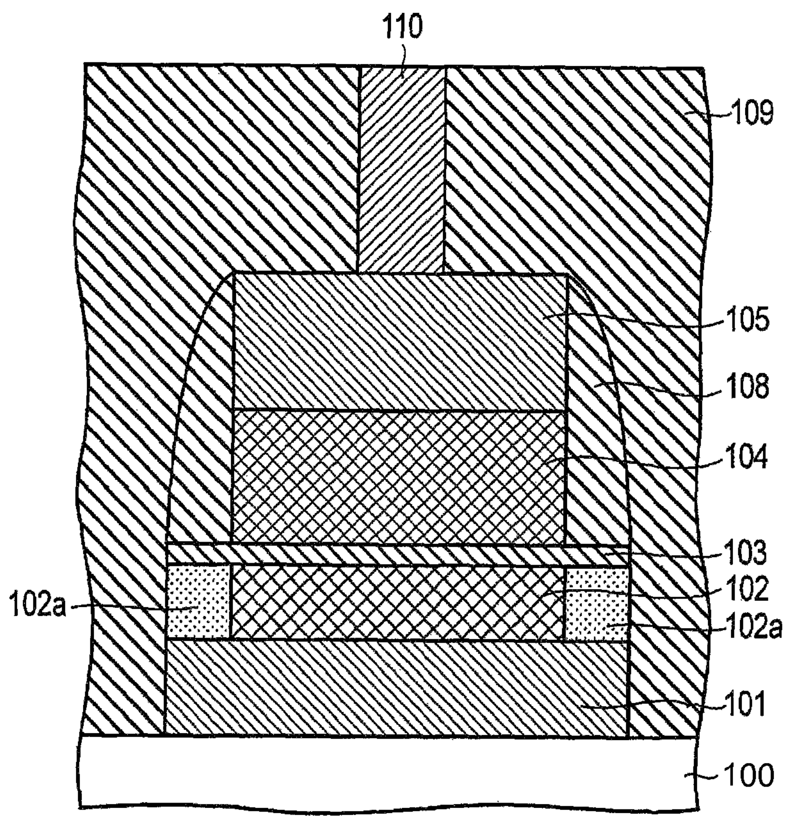

110
109
105
108
104
103
102a
102
102a
101
100

FIG. 9

MAGNETORESISTIVE ELEMENT AND METHOD OF MANUFACTURING THE SAME

CROSS-REFERENCE TO RELATED APPLICATIONS

This application claims the benefit of U.S. Provisional Application No. 61/876,081, filed Sep. 10, 2013, the entire contents of which are incorporated herein by reference.

FIELD

Embodiments described herein relate generally to a magnetoresistive element and a method of manufacturing the same.

BACKGROUND

In recent years, a semiconductor memory utilizing a resistance variable element as a memory element, such as a PRAM (phase-change random access memory) or an MRAM (magnetic random access memory), has been attracting attention and being developed. The MRAM is a device which performs a memory operation by storing “1” or “0” information in a memory cell by using a magnetoresistive effect, and has features of nonvolatility, high-speed operation, high integration and high reliability.

One of magnetoresistive effect elements is a magnetic tunnel junction (MTJ) element including a three-layer multilayer structure of a storage layer having a variable magnetization direction, an insulation film as a tunnel barrier, and a reference layer which maintains a predetermined magnetization direction.

The resistance of the MTJ element varies depending on the magnetization directions of the storage layer and the reference layer, it takes a minimum value when the magnetization directions are parallel, and takes a maximum value when the magnetization directions are antiparallel, and information is stored by associating the parallel state and antiparallel state with binary information “0” and binary information “1”, respectively.

The writing of information into the MTJ element involves a magnetic-field write scheme in which only the magnetization direction in the storage layer is reversed by a current magnetic field that is generated when a current flowing is flowed through a write line, and a write (spin injection write) scheme using spin angular momentum movement in which the magnetization direction in the storage layer is reversed by passing a spin polarization current through the MTJ element itself.

In the former scheme, when the element size is reduced, the coercivity of a magnetic body constituting the storage layer increases and the write current tends to increase, and thus it is difficult to achieve both the miniaturization and low electric current.

On the other hand, in the latter scheme (spin injection write scheme), spin polarized electron to be injected into the MTJ element decreases with the decrease of the volume of the magnetic layer constituting the storage layer, so that it is expected that both the miniaturization and low electric current may be easily achieved.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is a sectional view for explaining a manufacturing method of a magnetic memory according to a first embodiment.

FIG. **2** is a sectional view for explaining the manufacturing method of the magnetic memory according to the first embodiment following FIG. **1**.

FIG. **3** is a sectional view for explaining the manufacturing method of the magnetic memory according to the first embodiment following FIG. **2**.

FIG. **4** is a sectional view for explaining the manufacturing method of the magnetic memory according to the first embodiment following FIG. **3**.

FIG. **5** is a sectional view for explaining the manufacturing method according to the first embodiment following FIG. **4**.

FIG. **6** is a sectional view for explaining the manufacturing method according to the first embodiment following FIG. **5**.

FIG. **7** is a sectional view indicating an MRAM according to a second embodiment.

FIG. **8** is a sectional view for explaining a manufacturing method of a magnetic memory according to a third embodiment.

FIG. **9** is a sectional view for explaining the manufacturing method of the magnetic memory according to the third embodiment following FIG. **8**.

DETAILED DESCRIPTION

Embodiments will be hereinafter described with reference to the accompanying drawings. In the following drawings, portions corresponding to already-shown drawings will be denoted by the same signs (including a sign having a different subscript), and their detailed explanations will be omitted.

In general, according to one embodiment, a magnetoresistive element is disclosed. The magnetoresistive element includes a lower electrode; a stacked body provided on the lower electrode and including a first magnetic layer, a tunnel barrier layer and a second magnetic layer. The first magnetic layer includes a first region and a second region provided outside the first region to surround the first region. The second region includes an element included in the first region and other element being different from the element. A hard mask layer is provided on the stacked body. A cap layer is provided on the hard mask layer. The magnetoresistive element further includes an upper electrode penetrating the cap layer and contacting the hard mask.

According to an embodiment, a method for manufacturing a magnetoresistive element is disclosed. A stacked body is formed on a substrate. The stacked body includes a first magnetic layer, a tunnel barrier layer and a second magnetic layer. A hard mask layer is formed on the stacked body. A cap layer is formed on the hard mask layer. The cap layer is processed. The stacked body and the hard mask are etched using the processed cap layer as a mask. Ions are implanted into a portion of the stacked body that is outside of the cap layer using the cap layer as a mask.

First Embodiment

FIGS. **1** to **6** are sectional views for explaining a method of manufacturing a magnetic memory according to a first embodiment. In the present embodiment, a case where the magnetic memory is a magnetic random access memory (MRAM) will be described.

[FIG. **1**]

A lower electrode **101**, a storage layer **102**, a tunnel barrier layer **103**, a reference layer **104**, a hard mask **105** having conductivity and a cap layer **106** having insulating properties are successively formed on a substrate **100**.

The substrate **100** comprises a silicon substrate (semiconductor substrate), a selection transistor formed on a surface of the silicon substrate and configured to select an MTJ element, an interlayer insulating film, etc. The storage layer **102** comprises, for example, CoFeB. The tunnel barrier layer **103** comprises, for example, magnesium oxide (MgO). The reference layer **102** comprises, for example, an alloy of Pt (precious metal) and Ni or Co (magnetic material). The hard mask **105** comprises, for example, W, Ta or Ru. The cap layer **106** comprises, for example, silicon nitride.

[FIG. **2**]

The cap layer **106** is processed into a predetermined shape by etching the cap layer **106** using a resist pattern which is formed on the cap layer **106** and not shown as a mask.

[FIG. **3**]

The resist pattern and the cap layer **106** are used as a mask, and the hard mask **105** and the reference layer **104** are etched by RIE process. The RIE process is performed under the condition that it stops on the tunnel barrier layer **103**. The resist pattern disappears during the RIE process, and then the cap layer **106** functions as a mask of the etching.

Damage is caused on the storage layer **102** outside the cap layer **106** by the RIE process. The damage caused on the storage layer **102** may deteriorate magnetic anisotropy, spin injection efficiency and an MR ratio. Therefore, the damage may degrade the properties of the MTJ element.

It should be noted that the etching may be performed not only in RIE process but in IBE process.

[FIG. **4**]

In the present embodiment, ions **107** are implanted into the storage layer **102** using the cap layer **106** as a mask to reduce an influence of the damage of the storage layer **102**. In the figure, **102***a* denotes a storage layer of a portion into which the ions **107** are implanted (second region). The storage layer **102***a* includes, for example, CoFeB (magnetic material) and the ions **107** (element). The storage layer **102** (first region) under the cap layer **106** does not include the ions **107** (element).

The ions **107** are implanted also into the tunnel barrier layer **103** and the cap layer **106** on the storage layer **102***a*. The ions **107** may be implanted also into the lower electrode **101**.

The thickness of the cap layer **106** is selected in such a manner that the ions **107** are not to be implanted into the hard mask **105** when the ions are implanted into the tunnel barrier layer **103** and the storage layer **102***a*. For example, the thickness of the cap layer **106** is greater than the sum of the thickness of the tunnel barrier layer **103** and the thickness of the storage layer **102***a*. Thus, a problem that the ions **107** are implanted into the hard mask **105** and resistance of the hard mask **105** increases does not occur.

The reason why the influence of the damage of the storage layer **102** is reduced is that the storage layer **102***a* is demagnetized by ion implantation of the ions **107**. By the implantation of the ions **107**, the storage layer **102***a* is not only electrically deactivated, but it may be magnetically deactivated.

An element used as the ions **107** is, for example, at least one of As, Ge, Ga, Sb, In, N, Ar, He, F, Cl, Br, I, O, Si, B, C, Zr, Tb and Ti. Among them, especially, As and Ge are effective in reducing the influence of the damage of the storage layer **102**, since they have a large atomic radiuses. As and Ge may reduce a dose amount of the ion implantation.

[FIG. **5**]

An insulating layer is formed on an entire surface to cover the stacked body of the reference layer **104**, the hard mask **105** and the cap layer **106**, thereafter, a sidewall **108** comprising the insulating layer is formed on the side wall of the stacked body of the reference layer **104**, the hard mask **105** and the cap layer **106** by etching the entire surface of the insulating layer

[FIG. **6**]

The tunnel barrier layer **103**, the storage layer **102***a* and the lower electrode **101** are processed by etching using the sidewall **108** as a mask.

An insulating layer **109** is formed on an entire surface to cover the cap layer **106** and the sidewall **108**, thereafter, an opening reaching the hard mask **105** is formed in the insulating layer **109** and the cap layer **106**, and the upper electrode **110** is formed in this opening.

Since the ions **107** are not implanted into the hard mask **105** in the step of FIG. **4**, increase of contact resistance between the hard mask **105** and the upper electrode **110** is suppressed.

A process for forming the upper electrode **110** includes, for example, depositing conducting layer to be processed into the upper electrode **110** to fill in the opening, and then planarizing surfaces of the conducting layer and the insulating layer **109** by chemical mechanical polishing (CMP). As a result, the upper electrode **110** penetrating the cap layer **106** and contacting the hard mask **105** is obtained.

Second Embodiment

FIG. **7** is a sectional view for explaining an MRAM according to a second embodiment. The present embodiment is different from the first embodiment in a positional relationship between a storage layer **102** and a reference layer **104**, i.e., in that the storage layer **102** is arranged higher than the reference layer **104**.

The MRAM according to the present embodiment can be obtained in accordance with the manufacturing method according to the first embodiment, and has an advantage similar to that of the first embodiment. In FIG. **7**, **104***a* denotes a reference layer of a demagnetized portion into which ions **107** are implanted (fourth region). The reference layer **104***a* includes a magnetic material and the ions **107** (element). The reference layer **104** (third region) under a cap layer **106** does not include the ions **107** (element).

Third Embodiment

FIGS. **8** and **9** are sectional views for explaining a method of manufacturing an MRAM according to a third embodiment. In the present embodiment, a cap layer **106** is not formed.

A step of FIG. **8** corresponds to the step of FIG. **4** in the first embodiment (ion implantation).

In the present embodiment, the thickness of the hard mask **105** (D1) is set to be greater than the sum (D2) of the thickness of the tunnel barrier layer **103** and the thickness of the storage layer **102** (D1>D2).

Thus, if ions **107** are implanted into the tunnel barrier layer **103** and the storage layer **102** under the condition that the ions **107** are not implanted into a lower electrode **101**, a reference layer **104** is not damaged by the ions **107**, since the ions **107** implanted into the hard mask **105** do not reach the reference layer **104**.

Thereafter, the MRAM having a structure in which the upper electrode **110** shown in FIG. **9** contacts the hard mask **105** is obtained through steps similar to the steps of FIGS. **5** and **6** in the first embodiment.

The manufacturing method according to the above-described embodiments may be applied also to the MTJ element including a shift cancelling layer on the reference layer **104**. Although MTJ elements having various types of structures are present, the manufacturing methods according to the embodiments may be applied generally to a method of manufacturing an MTJ element including implanting an element into a magnetic layer to reduce the influence of the damage of the magnetic layer caused by the RIE process.

While certain embodiments have been described, these embodiments have been presented by way of example only, and are not intended to limit the scope of the inventions. Indeed, the novel methods and systems described herein may be embodied in a variety of other forms; furthermore, various omissions, substitutions and changes in the form of the methods and systems described herein may be made without departing from the spirit of the inventions. The accompanying claims and their equivalents are intended to cover such forms or modifications as would fall within the scope and spirit of the inventions.

What is claimed is:

1. A magnetoresistive element comprising:

a lower electrode;

a stacked body provided on the lower electrode and comprising a first magnetic layer, a tunnel barrier layer and a second magnetic layer, wherein the tunnel barrier layer is provided on the first magnetic layer, the second magnetic layer is provided on the tunnel barrier layer, the first magnetic layer comprises a first region and a second region provided outside the first region to surround the first region, and the second region comprises an element included in the first region and another element different from the element;

a hard mask layer provided on the stacked body;

a cap layer provided on the hard mask layer; and

an upper electrode penetrating the cap layer and contacting the hard mask layer.

2. The magnetoresistive element according to claim **1**, wherein the cap layer comprises the another element.

3. The magnetoresistive element according to claim **1**, wherein the first magnetic layer is a storage layer, and the second region of the first magnetic layer is demagnetized.

4. The magnetoresistive element according to claim **1**, wherein the first magnetic layer is a storage layer, the second magnetic layer is a reference layer, and widths of the storage layer and the tunnel barrier layer are greater than a width of the reference layer.

5. The magnetoresistive element according to claim **1**, wherein the another element is at least one of As, Ge, Ga, Sb, In, N, Ar, He, F, Cl, Br, I, O, Si, B, C, Zr, Tb and Ti.

6. The magnetoresistive element according to claim **1**, wherein the first magnetic layer is a reference layer, and the second magnetic layer is a storage layer.

7. The magnetoresistive element according to claim **1**, wherein the cap layer comprises silicon nitride.

* * * * *